Acct. No. 11-0224. Applicants further respectfully request that this response be accepted as a bona fide effort to meet any potential response requirements outstanding and due in the above captioned matter.

Please amend the application as follows:

IN THE SPECIFICATION:

Please substitute the paragraph in the specification bridging page 10 and 11 by the following:

--The communications board 20 comprises a self-contained CPU 22 (Hitachi 64 180 or a Zilog Z80 180) with the serial interface 32 disposed on the CPU side. The central processing unit CPU 22 has coordinated a fixed value memory storage 24 (read only memory ROM) of the type 27C 1000/2000 and a battery buffered operating data storage 25 (random access memory RAM) of the type DS 1225/1230Y. The connection between the central

processing unit CPU 22, the memory components 24, 25 and a serial communications controller 28 (Zilog Z85 C30) with the serial ports is performed by way of an address decoder 26 and an I/O decoder 27 and a bus. A serial port 29 of the communications controller 28 leads under connection of a power amplifier 30 (MAX483 or MAX487) to the display means 21 formed as a large display field, with which the temporary jackpot stand is displayed. An external personal-computer not illustrated is connectable at an interface 31 of the communications controller 28 formed as an RS 232 interface. An interface adapter 33 is connected at a serial interface 32 of the communications controller 28 formed as a serial interface RS 485. The interface adapter 33 comprises essentially an optical coupler 35 of the type 6 N 136 for galvanic separation and a power stage 34 disposed successively to the optical coupler 35. The network cabling 133 is connected to the power stage 34.--